What is Claimed is:

1. A video decoder comprising:

a memory having a bitstream buffer area and a frame memory area, with each area divided again according to a number of video bitstreams to be decoded, for storing a plurality of received video bitstreams to respective areas;

a single video decoding part for time multiplexing the plurality of video bitstreams received through the memory in fixed units, to decode the bitstreams, and storing respective areas of the memory;

a multi-display controlling part for assigning a display number to every display frame of the video bitstream according to a frame rate and a film mode, reading a data decoded in synchronization to a display synchronization signal from the memory and forwarding in a time multiplexing fashion, and reducing the display number after the data is forwarded; and,

a multi-decoding controlling part for determining a video bitstream to be decoded at the present time among the plurality of video bitstreams according to a display state of the multi-display controlling part, and forwarding the video bitstream to the single video decoding part.

2. A video decoder as claimed in claim 1, further comprising a sequence level header storage part having a plurality of sequence level header registers for the video bitstreams, for storing header information of the video bitstreams to respective sequence level header registers under the control of the multi-decoding controlling part.

3. A video decoder as claimed in claim 1, wherein the single video decoding part makes time multiplexing of the plurality of received video bitstreams in frames, and decodes

simultaneously under the control of the multi-display controlling part and the multi-decoding controlling part.

4. A video decoder as claimed in claim 1, wherein the multi-decoding controlling part determines a vid(dec_vid) of a frame to be decoded next upon completion of decoding one frame of a certain vid(vid denotes a video index, a number used for marking 'n' video bitstreams), wherein the next dec_vid is fixed if one of the following rules are met.

i) display of frames of the vid is completed already.

ii) the frame under display is required to be displayed once more and a source of the video bitstream is of progressive scanning.

iii) the frame under display is required to be displayed once more, a source of the video bitstream is of interlaced scanning, and a field parity is matched with disp_sync(disp_sync denotes a display frame synchronization).

5. A video decoder as claimed in claim 1, wherein the multi-display controlling part displays the same video bitstreams in one display synchronization less than two times, and a video bitstream to be displayed is determined in an order of a display number 1, a display number two or greater than 2, and a display number '0'.

6. A video decoder as claimed in claim 1, wherein the multi-display controlling part determines a field parity to be displayed at the present time is matched with a field parity of a display synchronization signal for each video bitstream, for not reducing the display number if the field parities are not matched.

7. A video decoder as claimed in claim 1, wherein the multi-display controlling part controls to determine match of a field parity to be displayed at the present time with a field parity of a display synchronization signal for each video bitstream, for repeating a prior field if the field parities are not matched.

8. A video decoder as claimed in claim 1, wherein the multi-display controlling part can make parallel processing if more than four frame memories are used for each of the bitstreams.

9. A method for decoding a video signal, comprising the steps of:

(1) time multiplexing a plurality of video bitstreams in frames, to decode the bitstreams;

(2) assigning a display number to every display frame of each of the video bitstreams according to a frame rate and a film mode, reading a data decoded in synchronization to a display synchronization signal from a memory and forwarding in a time multiplexing fashion, and reducing the display number; and,

(3) determining a video bitstream to be decoded at the present time among the plurality of video bitstreams according to a display state in the step (2).

10. A method as claimed in claim 9, wherein, in the step (2), the same video bitstream is displayed less than two times in one display synchronization, and a video bitstream to be displayed is determined in an order of a display number 1, a display number two or greater than 2, and a display number '0'.

11. A method as claimed in claim 9, wherein the step (2) includes the step of determining

a field parity to be displayed at the present time of being matched with a field parity of a display synchronization signal for each video bitstream, for not reducing the display number if the field parities are not matched.

12. A video decoder as claimed in claim 9, wherein the step (2) further includes the step of determining match of a field parity to be displayed at the present time with a field parity of a display synchronization signal for each video bitstream, for repeating a prior field if the field parities are not matched.

13. A video decoder as claimed in claim 9, wherein the step (2) further includes the step of decoding frames of the bitstream display of which is ended with reference to the display numbers of the bitstreams at a next time.

14. A video decoder as claimed in claim 9, wherein the step (2) further includes the step of decoding frames of the bitstream being displayed at the present time if display of the bitstream is required once more with reference to the display numbers of the bitstreams.

15. A video decoder as claimed in claim 14, wherein the step (2) further includes the step of decoding a next frame of the video bitstream only when a field parity to be displayed at the present time is matched with a field parity of a display synchronization signal for each video bitstream if a source of the video bitstream is of interlaced scanning.